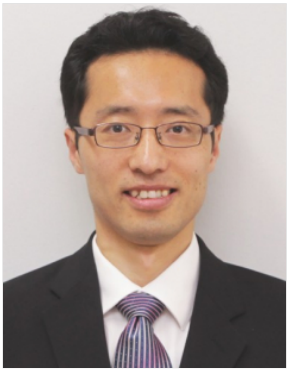

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Curriculum Vitae

2009.8-present: UNIST
2017.9-2018.8: Visiting professor at University of Toronto
2007.10-2009.8: Postdoc researcher at Arizona State University
2004.1-2007.10: Senior researcher at Samsung Electronics
2002.1-2003.4: Visiting scholar at Univ. of California-Irvine

Academic Credential

2004: Ph.D. in EECS from Seoul National University
1999: M.Sc. in EE from Seoul National University
1997: B.Sc. in EE from Seoul National University

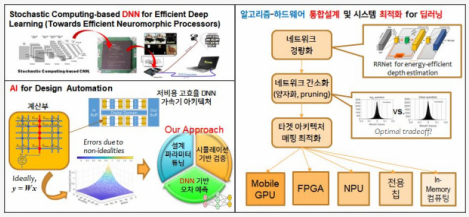
Awards/Honors/Memberships

Samsung HumanTech Award (2016)
Organizing committee / Program committee member:
LCTES 2019

ASP-DAC 2018
ICCAD 2017
ASP-DAC 2017
VLSI-SoC 2017
ICCAD 2016
KCS 2013-2017

Intelligent Computing and Codesign Lab
지능형 컴퓨팅 및 통합설계 연구실

Our research area is digital semiconductor design such as VLSI (Very Large Scale Integration) as well as processor architecture and compiler optimization. Through co-design of algorithm, hardware and software, we invent innovative techniques to optimize performance, power, cost and energy efficiency of emerging computer systems. Examples of such systems include AI (Artificial Intelligence) processors and Systems-on-Chips (SoCs) used for various applications.



우리 연구실의 주요 연구분야는 디지털 반도체 설계, 프로세서 아키텍처 및 컴파일러 등이며, 알고리즘-하드웨어-소프트웨어의 통합 설계를 통하여 시스템의 성능, 전력, 비용, 에너지 효율성 등을 최적화하는 기술들을 연구합니다. 대표적으로 인공지능(AI) 프로세서나 각종 응용에 사용되는 시스템온칩 등이 이러한 기법을 필요로 합니다.

관심분야

Algorithm-hardware-software co-design, AI and neural network processors, Electronic design automation, Architecture and compilers for embedded system.

희망분야

Algorithm-hardware-software co-design, AI and neural network processors, Electronic design automation, Architecture and compilers for embedded system.

Research Keywords and Topics

Deep learning processor architecture
Quantization methods for deep neural networks
Resistive Random Access Memory (ReRAM)
In-memory computing
Energy efficiency
Reconfigurable architecture
Compilers

Research Publications

- RRNet: Repetition-Reduction Network for Energy Efficient Depth Estimation, Sangyun Oh, Hye-Jin S. Kim, Jongeun Lee and Junmo Kim, IEEE Access, 8, pp. 106097-106108, IEEE, June, 2020.
- SparTANN: Sparse Training Accelerator for Neural Networks with Threshold-based Sparsification, Hyeonuk Sim, Jooyeon Choi and Jongeun Lee, Proc. of ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August, 2020.
- Learning to Predict IR Drop with Effective Training for ReRAM-based Neural Network Hardware, Sugil Lee, Mohammed Fouda, Jongeun Lee, Ahmed Eltawil and Fadi Kurdahi, Proc. of the 57th Annual ACM/IEEE Design Automation Conference (DAC), July, 2020.
- Cost-effective Stochastic MAC Circuits for Deep Neural Networks, Hyeonuk Sim and Jongeun Lee, Neural Networks, 117, pp. 152-162, Elsevier, September, 2019.

Patents

- 세밀한 정밀도 조정이 가능한 곱셈누적기, 이종은 외 1인, 대한민국 특허 10-2037043, 등록일 2019년 10월 22일.
- 반복 지수 양자화 기법 및 이를 이용한 딥뉴럴 네트워크 하드웨어 장치, 이종은 외 2인, 대한민국 및 미국 특허 출원중.